Chiplets
—How New Semiconductor Architectures Are Reshaping the Competitive Landscape—

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Why This Technology?

Entering 2024, a series of product announcements reflected advancements in chiplet technology, including Intel's (US) Gaudi 3, a semiconductor for generative AI, and Apple's (US) R1 chip for the Apple Vision Pro headset (manufactured by TSMC (Taiwan)).

With the release of the UCIe 2.0 specifications in August and support from key industry players such as ARM (UK), Intel, and TSMC, die-to-die and chip-to-chip connection standards have been established, lowering the barriers to adopting the technology, marking the beginning of its full-scale proliferation.

Summary

- The spread of chiplet technology is progressing, starting with high-performance computing, due to the balance between required functionality and cost.
- Chiplet technology is oriented toward development through standardization and cross-industry collaboration, leading to shifts in the supply chain and opportunities for non-linear growth for new entrants, particularly in design and front-end processes.

1. What is a Chiplet?

Chiplet is defined by IEEE[1] as a semiconductor industry standard as follows: "Chiplet is not a package type, it is part of a packaging architecture. It is an integrated circuit block that has been specifically designed to communicate with other chiplets, to form larger more complex ICs.[2]"[3] Since chiplets may be difficult to visualize by this definition alone, the following section provides additional context and explains the evolution leading up to chiplet technology.

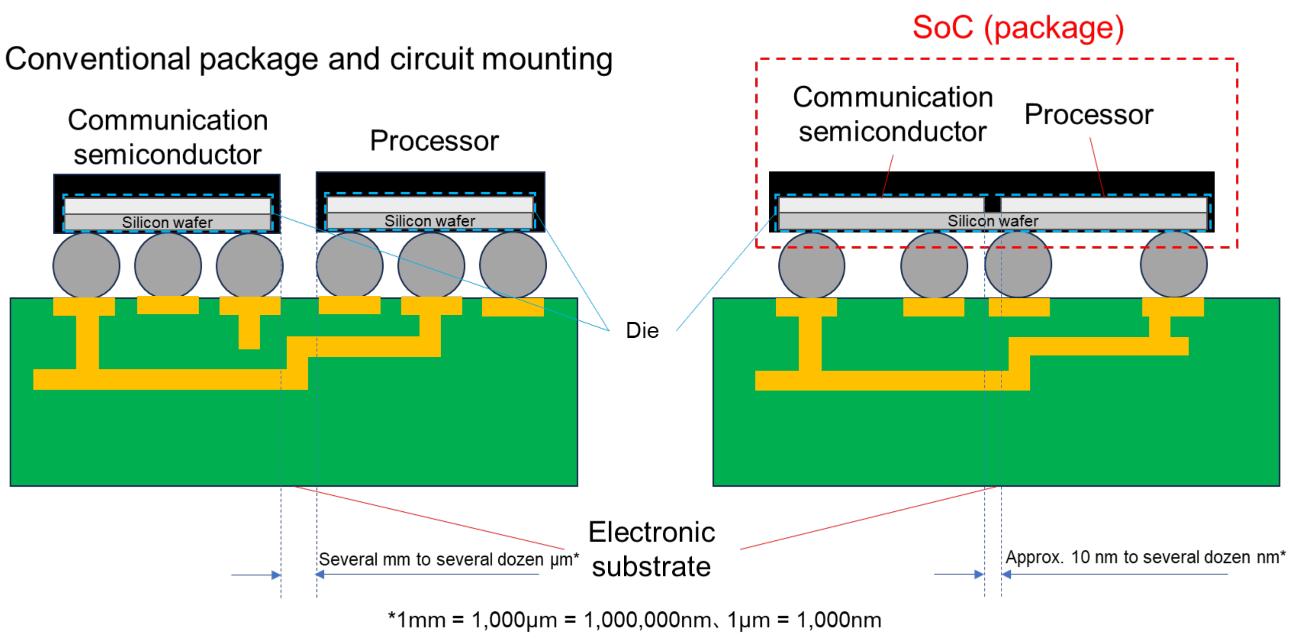
1-1. Semiconductor Integrated Circuit Blocks and SoCs[4]

A semiconductor integrated circuit block is a collection of circuits designed to perform a specific function. In conventional smartphones, semiconductors enable functions such as communication essential for network and phone use, data storage (memory), and information processing (processor).

[1] The Institute of Electrical and Electronics Engineers, Inc. This is the world's largest nonprofit organization for electrical and electronics professionals, dedicated to research in electronics and related fields.
[2] The Japan Electronics and Information Technology Industries Association (JEITA) defines a chiplet as "a silicon (Si) component, typically ranging in size from a few millimeters to several tens of millimeters square, on which transistors, diodes, resistors, capacitors, and other circuit elements are integrated and interconnected to function as an electronic circuit with a specific purpose." (tentative translation from Japanese source) This definition is adopted and used in this report.
[3] Chiplet Definition from the IEEE Electronics Packaging Society website
[4] System-on-Chip

For applications where size and communication latency are not major concerns, each semiconductor integrated circuit block is individually packaged and mounted on an electronic substrate (Figure 1, left). However, in smartphones and other applications requiring compact size and high-speed processing, semiconductor miniaturization has advanced to the point where the communication distance between circuit blocks (i.e., speed) has become a bottleneck to improve performance. This has created a need for greater integration of these functions. System-on-chip (SoC) technology became widely adopted to address this issue. SoCs integrate multiple semiconductor integrated circuit blocks with different functions onto a single silicon wafer (Figure 1, right).

Figure 1: Illustration of conventional packaging and mounted circuit, and SoC

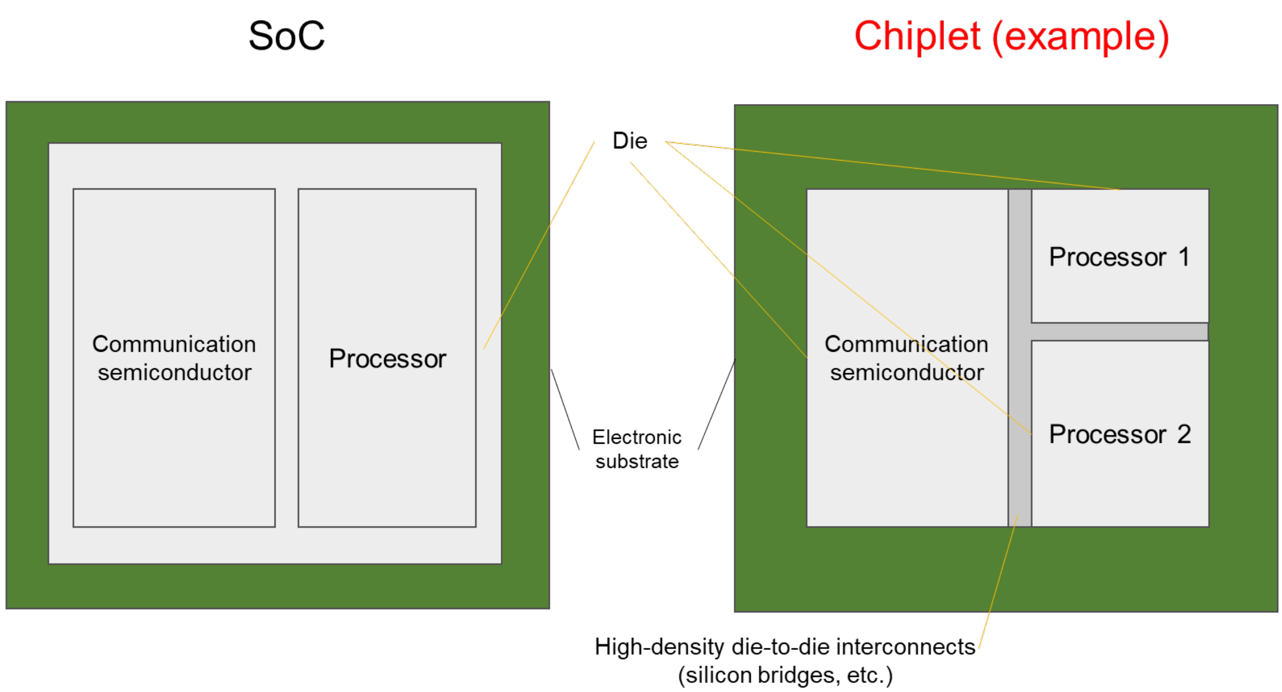


Source: Compiled by MGSSI based on various sources

1-2. From SoCs to Chiplets

While SoCs integrate all functions into a single die[5], chiplets take a modular approach by manufacturing separate dies for each function and connecting them with high-density interconnects on a scale comparable to SoC communications (Figure 2).

Figure 2: Illustration of SoC and chiplet

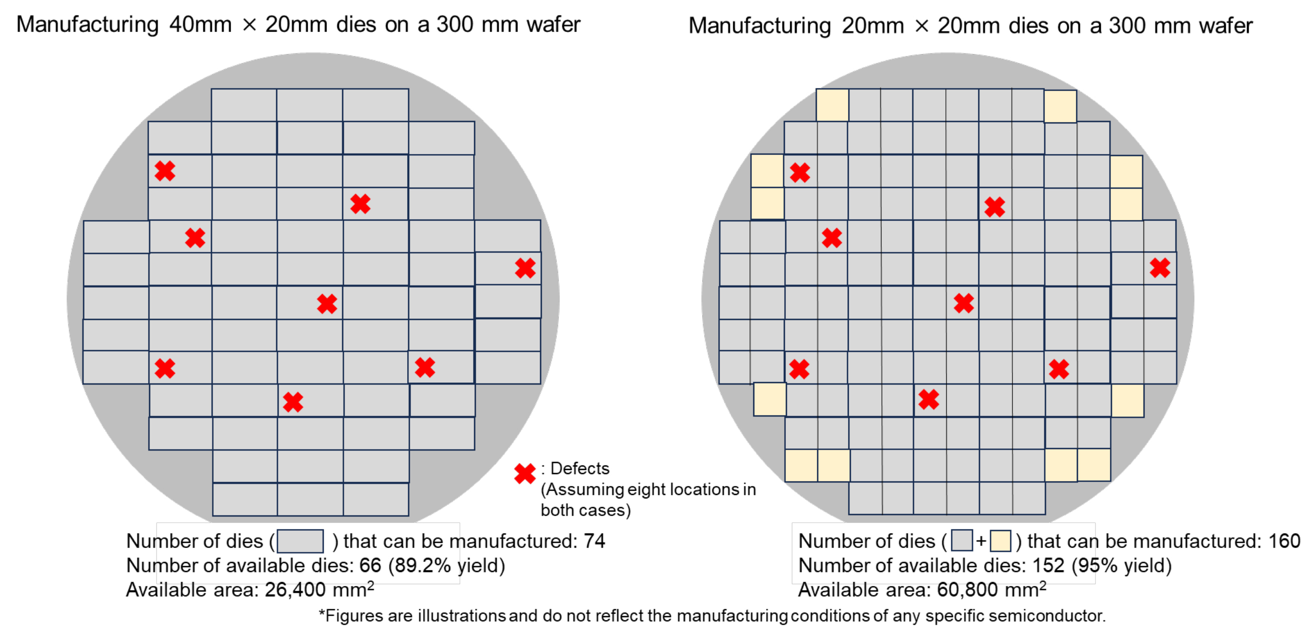


Source: Compiled by MGSSI based on various sources

[5] This report adopts the term die, a term that predates the emergence of chiplet technology. Intel refers to the dies that make up a chiplet as "tiles" (example). Meanwhile, IEEE, academia (example) etc. use the term "functional block" to contrast with chiplets, which are semiconductor integrated circuit blocks.

In the semiconductor industry, new technologies are only adopted if they provide cost-effective functionality. However, the benefits of miniaturization, which have historically driven both size and cost reduction, have been diminished by the rapid rise[6] in design and manufacturing costs. Additionally, the rapid spread of generative AI and the arrival of the CASE[7] era for automobiles have led to an increase in SoC sizes. This has introduced new challenges, including rising design costs, fewer dies per wafer reducing manufacturing efficiency, and a larger die area discarded per defect (Figure 3). Against this backdrop, chiplets, which involve manufacturing dies separately using the most suitable process for each function and then interconnecting them, are becoming advantageous in terms of both performance and cost.

Figure 3: Illustration of die size, number of dies per wafer, and yield loss due to defects



Source: Compiled by MGSSI based on various sources

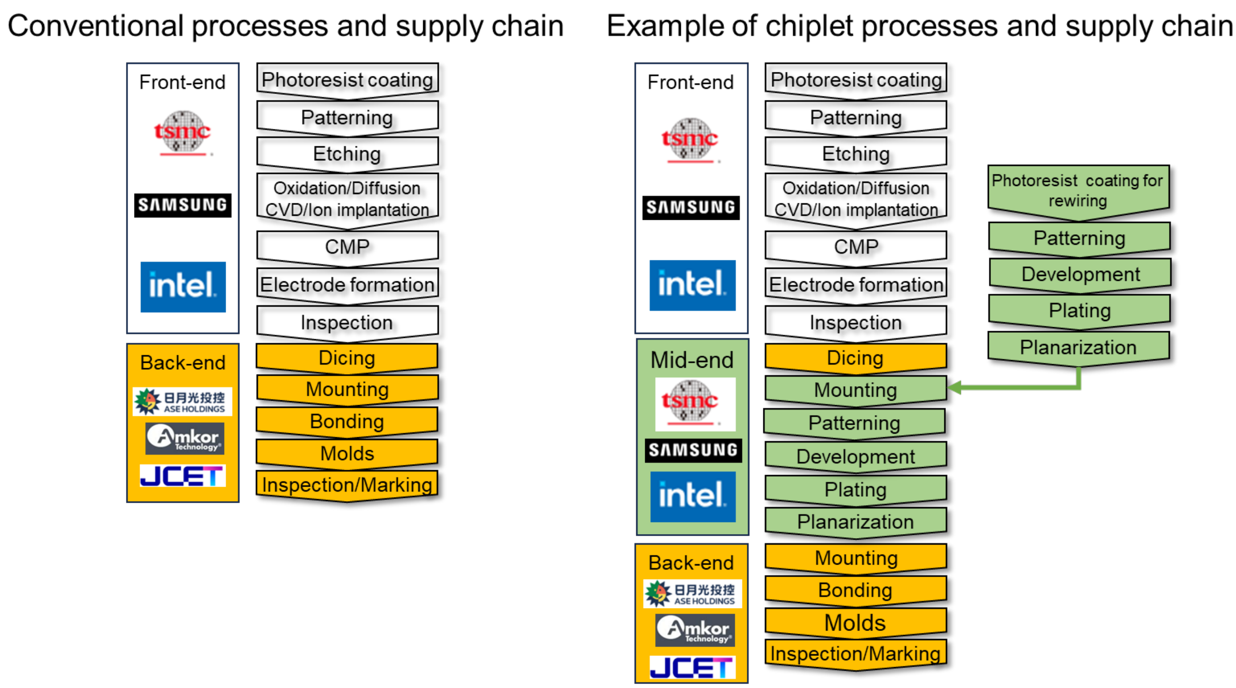
[6] A representative value is TSMC's price per wafer by process node (generation). See articles by Tech Power Up and Tom's Hardware for data. Data on design costs are available in Semiconductor Engineering.

[7] The emerging trend in the automotive industry for vehicles to be connected (wireless communication with the cloud and other vehicles), autonomous/automated, shared/service (mobility services and car-sharing), and electric.

1-3. Changes Brought About in Packaging Structure, Processes, and Supply Chain by Chiplets

Usually, each die cut from a wafer is encapsulated in resin or ceramic and electrically connected to external components via conductors such as pins in a later stage. In contrast, chiplet technology first establishes die-to-die electrical connections before encapsulation. As a result, new mid-end processes are required between the front-end and back-end processes, which were conventionally separated in semiconductor manufacturing (Figure 4). These mid-end processes are handled by front-end players such as TSMC, Samsung (South Korea), and Intel. In 2024, software vendors focusing on front-end processes, such as Cadence (US), moved to acquire CAE[8] software companies to support mid-end process design.

Figure 4: Process and supply chain changes due to chiplets



Source: Compiled by MGSSI based on various sources

2. Notable Trends

Established in 2022, the Universal Chiplet Interconnect Express (UCIe) Consortium released the UCIe 2.0 specifications in August 2024 to standardize die-to-die and chip-to-chip connections. With specifications now established for both horizontal and vertical (stacked) connections as well as for product management, the barriers to chiplet adoption have been significantly lowered, marking the beginning of widespread adoption. In addition to Intel, which has been at the forefront of launching related products, companies such as Cadence; the fabless

[8] CAE (Computer-Aided Engineering) is widely used in large-scale design fields larger than the semiconductor front-end process, such as mechanical and equipment engineering. CAE software is commonly used for simulations involving temperature changes due to heating and structural deformation under applied loads. On January 16, 2024, Synopsys (US) announced the acquisition of Ansys (US), and Cadence (US) announced its acquisition of BETA CAE (US) on March 5, 2024.

companies[9] AMD (US), ARM (UK), Alphawave Semi (UK), Global Unichip[10] (Taiwan), Google (US); and semiconductor testing equipment manufacturer Advantest (Japan) have issued statements in support of this advancement[11]. Alongside these eight companies, the growth of six startups that have also expressed support (Figure 5) is highly anticipated.

Figure 5: Notable startups in chiplet technology

Company name	Headquarters location	Overview	URL
Astera Labs	Santa Clara, California, US	Founded by Jitendra Mohan, Sanjay Gajendra, and Casey Morrison, formerly of Texas Instruments. A fabless company that provides technology to maintain and streamline data flow for data centers. Selected as one of the "Next Billion-Dollar Startups" in 2022.	https://www.asteralabs.com/
Ayar Labs	San Jose, California, US	A fabless company that has developed TeraPHY™, a chiplet for optical data transfer. By integrating optical communication within the chiplet, it claims to achieve 5–10 times the bandwidth of conventional data transfer. It also reduces latency to one-tenth while consuming one-quarter to one-eighth of the power. Nvidia has invested in this company.	https://ayarlabs.com/
Blue Cheetah	Sunnyvale, California, US	Offers the BlueLynx D2D IP, which flexibly supports chip-to-chip interconnects for 16nm to 3nm process nodes. Tom Kelly, the company's COO, is among several members from Cadence's analog division.	https://www.bcanalog.com/
Eliyan	Santa Clara, California, US	Developed NuLink™, a technology that enables high-speed chiplet interconnects on standard organic substrates without using an interposer. Completed designs for 5 nm and 3 nm process nodes and offering IP solutions.	https://eliyan.com/
eTopus	San Jose, California, US	Offers ePHY™, a solution for minimizing data transfer losses at different data transfer and interconnect points for data centers, 5G communications, and enterprise IT infrastructure.	https://etopus.com/
Kandou Bus	Saint-Sulpice (suburb of Lausanne), Switzerland	Provides technology to minimize data transfer errors and latency between electronic components. Offers high-speed transmission technologies for the latest USB standards and PCIe, a high-speed transmission standard for external memory, etc., as well as Glasswing™ IP, which enables highly efficient interconnections between electronic components in AR/VR glasses.	https://kandou.com/about/

Source: Compiled by MGSSI based on company websites

3. Future Prospects

The first-generation chiplet technology, which connects CPU and GPU dies, memory, and multiple dies using silicon interconnects, is already being adopted in high-performance computing semiconductors[12], including those for generative AI by Nvidia (US), AMD (US), and Intel (US). As die interconnects transition from the current 16nm to 12nm process to the 7nm process, the industry is expected to shift toward "ghiplets," a model in which GPUs are functionally partitioned and manufactured as chiplets[13].

Within five years, chiplet adoption in automotive semiconductors is also expected to begin. Advanced SoC Research for Automotive (ASRA)[14] is developing automotive semiconductors that apply chiplet technology, aiming

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[9] A fabless semiconductor company designs and sells semiconductor products or licenses intellectual property (IP) relying on contract manufacturers, without owning its own manufacturing facilities. Companies that specialize exclusively in licensing IP are referred to as IP vendors/partners, but for simplicity, this report includes them under the term fabless.

[10] Taiwan Semiconductor Manufacturing Company (TSMC) is its largest shareholder. Leveraging a close partnership with TSMC, it leads the industry in design using cutting-edge process and packaging technologies.

[11] See to the UCIe Consortium website for official statements from each company: https://www.uciexpress.org/_files/ugd/0c1418_74c8a7bba0714b489dd54ef658c1c968.pdf

[12] From the release of the GP100 graphics processor incorporating a GPU for VR and AI applications in 2016, to the Blackwell GPU, announced in March 2024 and specialized for generative AI, Nvidia has adopted TSMC's chip on wafer on substrate (CoWoS) technology, which connects GPU and memory (HBM) via a silicon interposer. AMD's Instinct MI300 series, a GPU released in December 2023, also utilizes CoWoS. Intel's Gaudi 3, a chip announced in April 2024 for AI training, employs embedded multi-die integrated bridge (EMIB) technology, where two dies are connected via a silicon bridge, allowing them to function as a single chip.

[13] Intel's Ponte Vecchio GPU, announced in September 2022 for high-performance computing, is considered a benchmark ghiplet product, integrating 47 dies within a single package using EMIB and 3D interconnects. This approach is based on a balance between efficient utilization of 7nm EUV lithography and the costs associated with die scaling and miniaturization.

[14] Established on December 1, 2023, the organization currently comprises Subaru (Japan), Toyota (Japan), Nissan (Japan), Honda (Japan), Mazda (Japan), Denso (Japan), Panasonic Automotive Systems (Japan), Socionext Inc. (Japan), Cadence Design Systems, Japan (Japan), Nihon Synopsys (Japan), Mirise Technologies (Japan), and Renesas Electronics (Japan).

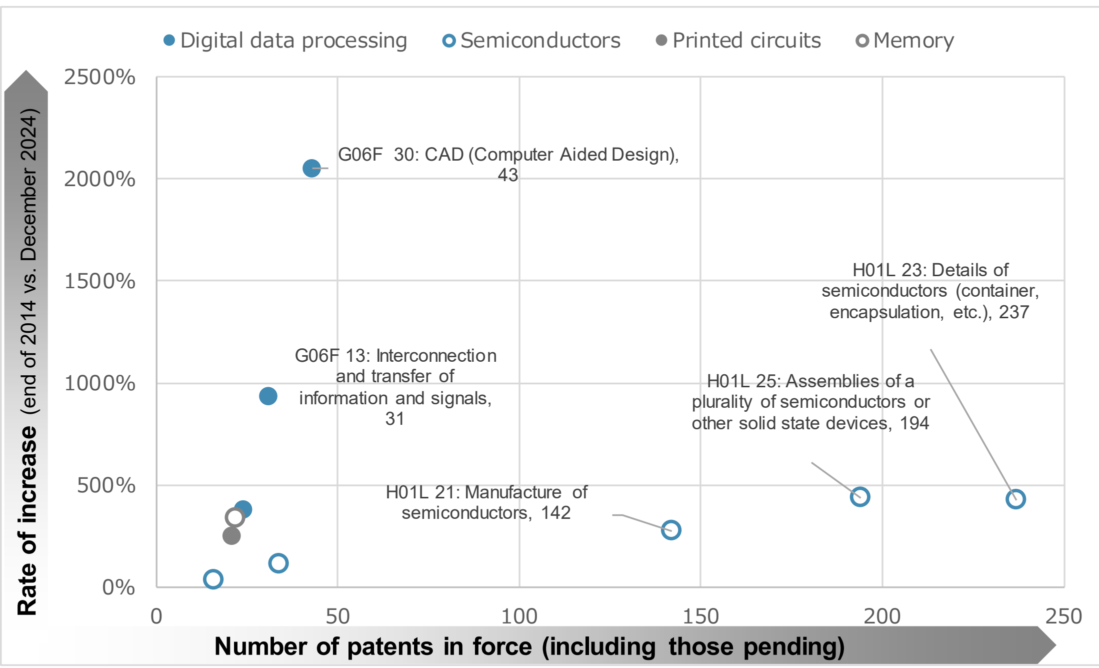
for installation in mass-produced vehicles from 2030. Chiplet technology is also anticipated to play an important role in the advancement of CASE vehicles.

IP Analysis of Chiplets

Keywords such as "chiplet" that are closely related to this technology and International Patent Classification (IPC) codes associated with semiconductors and computer aided design (CAD) were identified (289 in force as of December 2024, including pending applications[15]) and an analysis was conducted based on technology classifications and top players.

Figure 6 compares the number of patents in force chiplets and their growth rates. The horizontal axis represents the number of patents in force, while the vertical axis shows the growth rate by comparing the number of patents in force as of December 2024 with those at the end of 2014. These results indicate a growing focus on details of semiconductors (H01L30) and module-related technologies (H01L25). In recent years, there has also been a significant increase in the number of patents related to design tools (electronic design automation: EDA) classified under CAD (G06F30).

Figure 6: Number of patents in force and growth rate (by technology category)

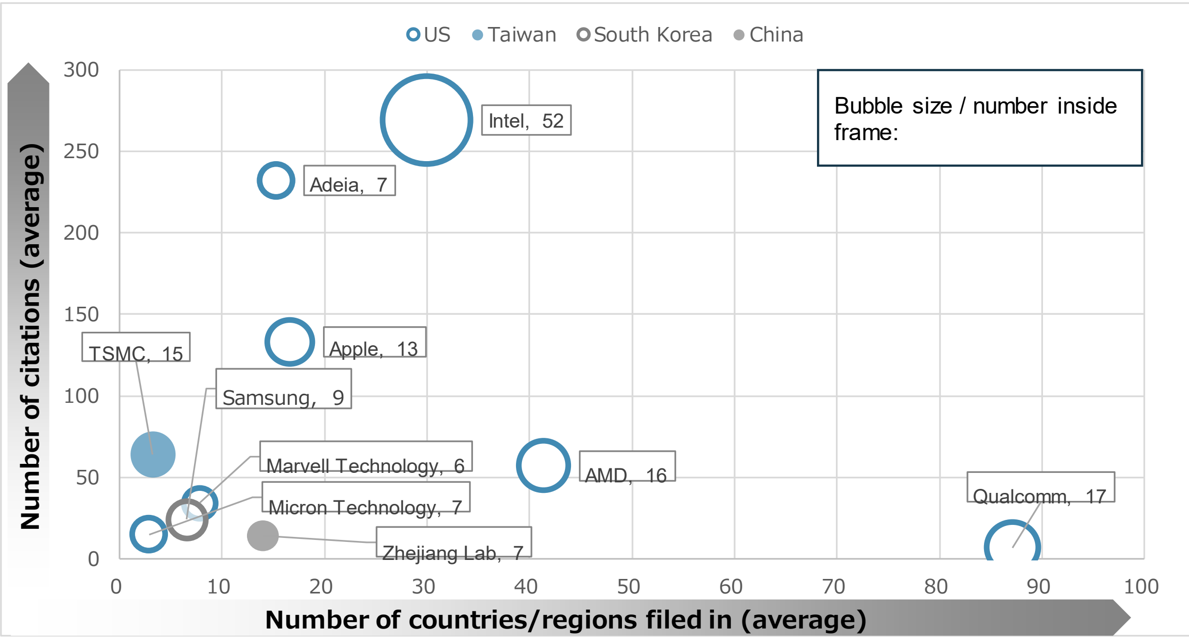


Source: Compiled by MGSSI based on data from LexisNexis PatentSight

[15] The total number of patents includes both filed patents and granted patents that have completed the examination process and are enforceable as intellectual property rights.

Figure 7 compares the top players in terms of the number of patents related to chiplets. The bubble size represents the number of patents in force, the horizontal axis indicates the average number of countries or regions where applications were filed, and the vertical axis represents the average number of citations, reflecting the technological impact. The results show that US companies dominate the top ranks, highlighting their significant influence in chiplet technology. Leading the field by a considerable margin, Intel has filed seven patents since 2022 that are highly relevant to the UCIe standard, as they explicitly mention "Universal Chiplet Interconnect Express" or "UCIe" in their documentation. Although all these patents are still under review, they reflect Intel's strong commitment to this technology.

Figure 7: Number of patents in force, number of countries/regions filed in, and number of citations (by top players)



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